QP Code : 30666

(3 Hours)

Max Marks: 80

1. Question No. 1 is compulsory.
2. Out of remaining questions, attempt any three questions.
3. Assume suitable additional data if required.
4. Figures in brackets on the right hand side indicate full marks.

1.	(A)	Compare Combinational circuits with Sequential circuits.	(05)
	(B)	Compare Synchronous with Asynchronous counter.	(05)
	(C)	Compare TTL with CMOS logic families.	(05)
	(D)	Compare PLA with PAL.	(05)

2. (A) Write the VHDL code for 2-bit up-down counter with positive edge triggered clock.   (10)
   (B) State and prove the De Morgan's theorem.   (05)
   (C) Draw the block diagram of internal architecture of XC4000 family FPGA.   (05)

3. (A) Design synchronous counter using T-type flip flops for getting the following sequence: $0 \to 2 \to 4 \to 6 \to 0$. Take care of lockout condition.   (10)
   (B) Convert T-type flip flop into D-type flip flop.   (05)
   (C) Write $(AB)_{16}$ into its BCD code and Octal code.   (05)

4. (A) Implement the following Boolean equation using single 4:1 MUX and few logic gates: (10)
   $$F(P,Q,R,S) = \prod M(0, 2, 5, 6, 7, 9, 12, 15).$$
   (B) Compare FPGAs with CPLDs.   (05)
   (C) Implement $Y = A + \overline{B} C$ using only NOR gates.   (05)

5. (A) Draw a neat circuit of BCD adder using IC 7483 and explain.   (10)
   (B) Using Quine McClusky method, minimize the following: (10)
   $$F(P,Q,R,S) = \sum m(0,1,3,7,8,9,15) + d(2,10,11).$$

6. (A) Design a Mealy type sequence detector circuit to detect a sequence 1101 using T-type flip flops.   (10)
   (B) What is shift register? Explain any one type of shift register. Give its application.   (10)

=============